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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <small>(use as many sheets as necessary)</small>		Application Number	10/667,615
		Filing Date	09/22/03
		First Named Inventor	Theodore W. Houston
		Group Art Unit	2811
		Examiner Name	Douglas W. Owens
Sheet	1	of	1
		Attorney Docket No.	TI-35657

U.S. PATENT DOCUMENTS

Exam. Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
RMJ	AA	6,396,108		Krivokapic et al.	5/28/02	
QMJ	AB	6,307,230		Chatterjee et al.	10/23/01	
WJM	AC	6,225,175		Houston	5/1/01	
	AD					
	AE					
	AF					
	AG					
	AH					
	AI					
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	AK					
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FOREIGN PATENT DOCUMENTS

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Exam. Initials*	Cite No. ¹	Foreign Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴				
DRP	BA	WO	02/103703 A2	Innovative Silicon SA	12/27/02		
	BB						
	BC						
	BD						
	BE						
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

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Exam. Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>DWJ</i>	CA	KAZUMI INOH, ET AL., "FBC (Floating Body Cell) for Embedded DRAM on SOI" 2003 Symposium on VLSI Technology Digest of Technical Papers, pp. 1-2	
<i>DWJ</i>	CB	TAKASHI OHSAWA, ET AL., "A Memory Using One-Transistor Gain Cell on SOI (FBC) with Performance Suitable for Embedded DRAM's" 2003 Symposium on VLSI Circuits Digest of Technical Papers, pp. 1-4	
<i>DWJ</i>	CC	B. DOYLE, ET AL., "Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout" 2003 Symposium on VLSI Technology Digest of Technical Papers, pp. 1-2	
	CD		
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